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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,440	02/10/2004	Jeffrey P. Gambino	FIS920020146US2 (15928A)	9422
23389	7590	04/13/2006	EXAMINER PHAM, HOAI V	
SCULLY SCOTT MURPHY & PRESSER, PC 400 GARDEN CITY PLAZA SUITE 300 GARDEN CITY, NY 11530			ART UNIT 2814	PAPER NUMBER

DATE MAILED: 04/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/775,440

Applicant(s)

GAMBINO ET AL.

Examiner

Hoai v. Pham

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 16-18,20 and 21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 16-18,20 and 21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 16 is rejected under 35 U.S.C. 102(b) as being anticipated by Pan [U.S. Pat. 5,599,726] newly cited.

Pan (fig. 3, cols. 4-6) discloses a MOSFET device comprising a silicon substrate (10) having a shallow trench isolation (12a, 12b), a gate dielectric (14) and a gate stack (16) located on the silicon substrate (10), and a fluorine doped low K dielectric oxide gate spacers (18) located on sidewalls of the gate stack (16), the fluorine doped low K dielectric oxide gate spacers (18) having a fluorine content of about $1\text{E}14$ to $1\text{E}16\text{ cm}^{-2}$ (see col. 6, lines 38-41).

3. Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by Kasai [U.S. Pat. 5,973,371] newly cited.

Kasai (fig. 7, cols. 6, 8, and 11-12) discloses a MOSFET device comprising a silicon substrate having shallow trench isolation STI (22) located therein, a gate dielectric (24) and a gate stack (25) located on said silicon substrate, a fluorine doped low K dielectric oxide gate spacer (27) (see col. 6, lines 62-67) located on sidewalls of

said gate stack, and a silicon nitride oxide layer (26) (see col. 6, lines 56-61) located on at least said gate stack (25).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan [U.S. Pat. 5,599,726] newly cited.

Aminpur does not explicitly disclose the dielectric constant value as claimed by Applicant. However, the dielectric constant value range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal

or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

7. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horstman et al. [U.S. Pat. 6,555,829] newly cited, in view of Pan [U.S. Pat. 5,599,726] newly cited.

With respect to claim 16, Horstman et al. (fig. 2a, cols. 4-6) discloses a MOSFET device comprising a silicon substrate (201) having a shallow trench isolation (202), a gate dielectric (203) and a gate stack (204) located on the silicon substrate (201), and a fluorine doped low K dielectric oxide gate spacers (207) located on sidewalls of the gate stack (204).

Horstman et al. does not explicitly disclose the fluorine doped low K dielectric oxide gate spacers having a fluorine content of about $1\text{E}14$ to $1\text{E}16\text{ cm}^{-2}$. However, Pan discloses the fluorine doped low K dielectric oxide gate spacers (18) having a fluorine content of about $1\text{E}14$ to $1\text{E}16\text{ cm}^{-2}$ (see col. 6, lines 38-41). Moreover, the fluorine range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected

results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Therefore, it would have been obvious to one having ordinary skill in the art to dope the fluorine with content of about $1\text{E}14$ to $1\text{E}16\text{ cm}^{-2}$ in the oxide gate spacers as taught by Pan into the process of Horstman et al. because the doping of fluorine would reduce parasitic capacitances to the MOSFET (see col. 6, lines 28-33).

With respect to claims 17-18, Horstman et al. discloses that the fluorine doped low K dielectric oxide gate spacer (207) having a dielectric constant value in the range of 2.6 to 3.5 (see col. 5, lines 14-15). Horstman et al. does not explicitly disclose the dielectric constant value as claimed by Applicant. However, the dielectric constant value range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is

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aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horstman et al. [U.S. Pat. 6,555,829] newly cited, in view of Pan [U.S. Pat. 5,599,726] newly cited, as applied to claim 16 above, and further in view of Kasai [U.S. Pat. 5,973,371] newly cited.

Horstman et al. does not disclose a silicon nitride oxide layer located on at least the gate stack. However, Kasai discloses a silicon nitride oxide layer (26) formed over the MOSFET device (see col. 6, lines 56-61). Therefore, it would have been obvious to one having ordinary skill in the art to form silicon nitride oxide layer over the MOSFET device as taught by Kasai into the device of Horstman et al. in order to protect the gate stack since silicon nitride oxide layer is good insulating characteristics.

Response to Arguments

9. Applicant's arguments with respect to claims 16-18, 20 and 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



HOAI PHAM
PRIMARY EXAMINER